



GENERAL DESCRIPTION

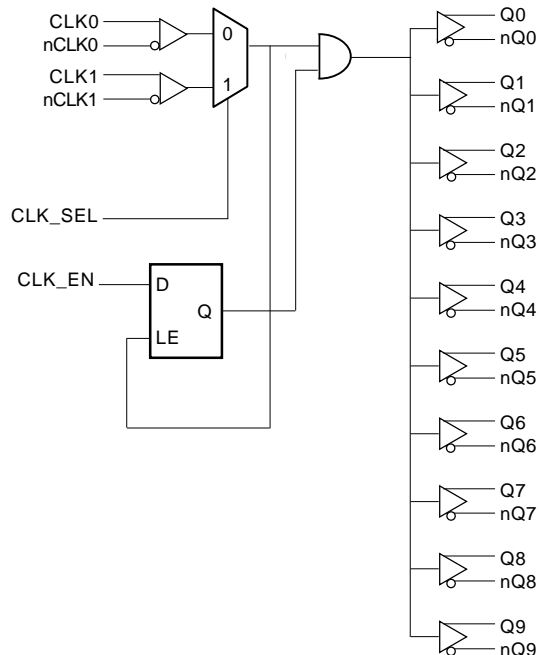


The ICS85310I-11 is a low skew, high performance 1-to-10 Differential-to-2.5V/3.3V ECL/LVPECL Fanout Buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The CLKx, nCLKx pairs can accept most standard differential input levels. The ICS85310I-11 is characterized to operate from either a 2.5V or a 3.3V power supply. Guaranteed output and part-to-part skew characteristics make the ICS85310I-11 ideal for those clock distribution applications demanding well defined performance and repeatability.

FEATURES

- 10 differential 2.5V/3.3V LVPECL/ECL outputs
- 2 selectable differential input pairs
- CLKx, nCLKx pairs can accept the following differential input levels: LVDS, LVPECL, LVHSTL, SSTL, HCSL
- Maximum output frequency: 700MHz
- Translates any single ended input signal to 3.3V LVPECL levels with resistor bias on nCLK input
- Output skew: 30ps (typical)
- Part-to-part skew: 140ps (typical)
- Propagation delay: 2ns (typical)
- LVPECL mode operating voltage supply range: $V_{CC} = 2.375V$ to $3.8V$, $V_{EE} = 0V$
- ECL mode operating voltage supply range: $V_{CC} = 0V$, $V_{EE} = -2.375V$ to $-3.8V$
- $-40^{\circ}C$ to $85^{\circ}C$ ambient operating temperature

BLOCK DIAGRAM



PIN ASSIGNMENT

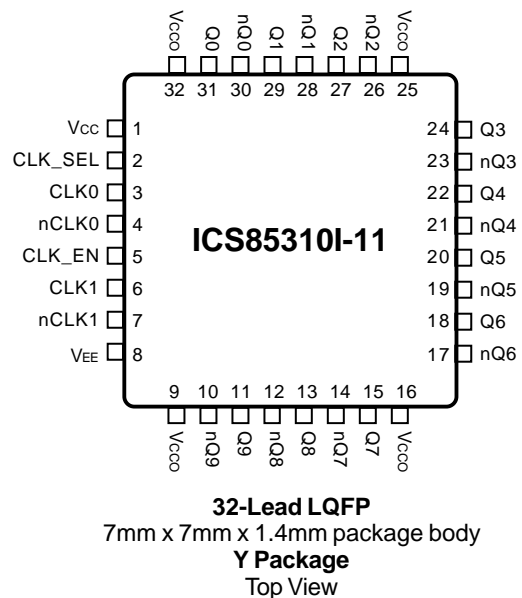




TABLE 1. PIN DESCRIPTIONS

| Number | Name | Type | | Description |
|---------------|------------------|--------|----------|--|
| 1 | V _{CC} | Power | | Core supply pin. |
| 2 | CLK_SEL | Input | Pulldown | Clock select input. When HIGH, selects CLK1, nCLK1 inputs. When LOW, selects CLK0, nCLK0 inputs. LVCMOS / LVTTTL interface levels. |
| 3 | CLK0 | Input | Pulldown | Non-inverting differential clock input. |
| 4 | nCLK0 | Input | Pullup | Inverting differential clock input. |
| 5 | CLK_EN | Input | Pullup | Synchronizing clock enable. When HIGH, clock outputs follow clock input. When LOW, Q outputs are forced low, nQ outputs are forced high. LVCMOS / LVTTTL interface levels. |
| 6 | CLK1 | Input | Pulldown | Non-inverting differential clock input. |
| 7 | nCLK1 | Input | Pullup | Inverting differential clock input. |
| 8 | V _{EE} | Power | | Negative supply pin. |
| 9, 16, 25, 32 | V _{CCO} | Power | | Output supply pins. |
| 10, 11 | nQ9, Q9 | Output | | Differential output pair. LVPECL interface levels. |
| 12, 13 | nQ8, Q8 | Output | | Differential output pair. LVPECL interface levels. |
| 14, 15 | nQ7, Q7 | Output | | Differential output pair. LVPECL interface levels. |
| 17, 18 | nQ6, Q6 | Output | | Differential output pair. LVPECL interface levels. |
| 19, 20 | nQ5, Q5 | Output | | Differential output pair. LVPECL interface levels. |
| 21, 22 | nQ4, Q4 | Output | | Differential output pair. LVPECL interface levels. |
| 23, 24 | nQ3, Q3 | Output | | Differential output pair. LVPECL interface levels. |
| 26, 27 | nQ2, Q2 | Output | | Differential output pair. LVPECL interface levels. |
| 28, 29 | nQ1, Q1 | Output | | Differential output pair. LVPECL interface levels. |
| 30, 31 | nQ0, Q0 | Output | | Differential output pair. LVPECL interface levels. |

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------------------|-------------------------|-----------------|---------|---------|---------|-------|
| C _{IN} | Input Capacitance | | | | 4 | pF |
| R _{PULLUP} | Input Pullup Resistor | | | 51 | | KΩ |
| R _{PULLDOWN} | Input Pulldown Resistor | | | 51 | | KΩ |



TABLE 3A. CONTROL INPUT FUNCTION TABLE

| Inputs | | Outputs | |
|--------|-----------------|---------------|----------------|
| CLK_EN | Selected Source | Q0:Q9 | Q0:Q9 |
| 0 | CLK0, nCLK0 | Disabled; LOW | Disabled; HIGH |
| 1 | CLK1, nCLK1 | Enabled | Enabled |

After CLK_EN switches, the clock outputs are disabled or enabled following a rising and falling input clock edge as shown in Figure 1.

In the active mode, the state of the outputs are a function of the CLK0, nCLK0 and CLK1, nCLK1 inputs as described in Table 3B.

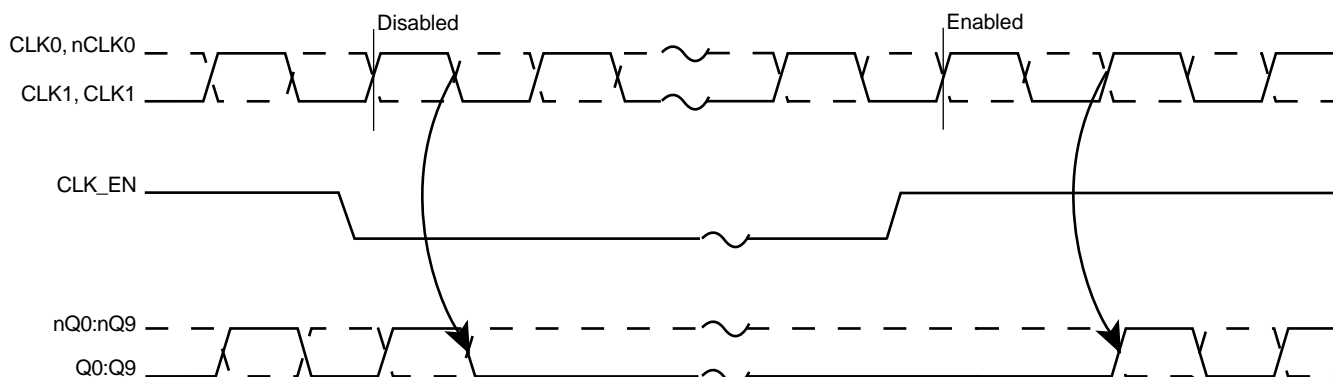


FIGURE 1. CLK_EN TIMING DIAGRAM

TABLE 3B. CLOCK INPUT FUNCTION TABLE

| Inputs | | Outputs | | Input to Output Mode | Polarity |
|----------------|----------------|---------|--------|------------------------------|---------------|
| CLK0 or CLK1 | nCLK0 or nCLK1 | Q0:Q9 | nQ0:Q9 | | |
| 0 | 1 | LOW | HIGH | Differential to Differential | Non Inverting |
| 1 | 0 | HIGH | LOW | Differential to Differential | Non Inverting |
| 0 | Biased; NOTE 1 | LOW | HIGH | Single Ended to Differential | Non Inverting |
| 1 | Biased; NOTE 1 | HIGH | LOW | Single Ended to Differential | Non Inverting |
| Biased; NOTE 1 | 0 | HIGH | LOW | Single Ended to Differential | Inverting |
| Biased; NOTE 1 | 1 | LOW | HIGH | Single Ended to Differential | Inverting |

NOTE 1: Please refer to the Application Information, "Wiring the Differential Input to Accept Single Ended Levels".



ABSOLUTE MAXIMUM RATINGS

| | |
|--|---------------------------|
| Supply Voltage, V_{CC} | 4.6V |
| Inputs, V_{CC} | -0.5V to $V_{CC} + 0.5V$ |
| Outputs, V_{CCO} | -0.5V to $V_{CCO} + 0.5V$ |
| Package Thermal Impedance, θ_{JA} | 47.9°C/W (0 lfpm) |
| Storage Temperature, T_{STG} | -65°C to 150°C |

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{CC} = V_{CCO} = 2.375V$ TO $3.8V$, $T_A = -40^\circ C$ TO $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|-----------------------|-----------------|---------|---------|---------|-------|
| V_{CC} | Core Supply Voltage | | 2.375 | 3.3 | 3.8 | V |
| V_{CCO} | Output Supply Voltage | | 2.375 | 3.3 | 3.8 | V |
| I_{EE} | Power Supply Current | | | | 120 | mA |

Table 4B. LVCMOS/LVTTL DC Characteristics, $V_{CC} = V_{CCO} = 2.375V$ TO $3.8V$, $T_A = -40^\circ C$ TO $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|----------|--------------------|--------------------|------------------------------|---------|----------------|---------|
| V_{IH} | Input High Voltage | CLK_SEL, CLK_EN | 2 | | $V_{CC} + 0.3$ | V |
| V_{IL} | Input Low Voltage | CLK_SEL, CLK_EN | -0.3 | | 0.8 | V |
| I_{IH} | Input High Current | CLK_EN | $V_{CC} = V_{IN} = 3.8V$ | | 5 | μA |
| | | CLK_SEL | $V_{CC} = V_{IN} = 3.8V$ | | 150 | μA |
| I_{IL} | Input Low Current | CLK_EN | $V_{CC} = 3.8V, V_{IN} = 0V$ | -150 | | μA |
| | | CLK_SEL | $V_{CC} = 3.8V, V_{IN} = 0V$ | -5 | | μA |

TABLE 4C. DIFFERENTIAL DC CHARACTERISTICS, $V_{CC} = V_{CCO} = 2.375V$ TO $3.8V$, $T_A = -40^\circ C$ TO $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|--------------------------------------|-----------------|------------------------------|---------|-----------------|---------|
| I_{IH} | Input High Current | CLK0, CLK1 | $V_{CC} = V_{IN} = 3.8V$ | | 150 | μA |
| | | nCLK0, nCLK1 | $V_{CC} = V_{IN} = 3.8V$ | | 5 | μA |
| I_{IL} | Input Low Current | CLK0, CLK1 | $V_{CC} = 3.8V, V_{IN} = 0V$ | -5 | | μA |
| | | nCLK0, nCLK1 | $V_{CC} = 3.8V, V_{IN} = 0V$ | -150 | | μA |
| V_{PP} | Peak-to-Peak Input Voltage | | 0.15 | | 1.3 | V |
| V_{CMR} | Common Mode Input Voltage; NOTE 1, 2 | | $V_{EE} + 0.5$ | | $V_{CC} - 0.85$ | V |

NOTE 1: Common mode voltage is defined as V_{IH} .

NOTE 2: For single ended applications, the maximum input voltage for CLK0, nCLK0 and CLK1, nCLK1 is $V_{CC} + 0.3V$.



TABLE 4D. LVPECL DC CHARACTERISTICS, $V_{CC} = V_{CCO} = 2.375V$ TO $3.8V$, $T_A = -40^{\circ}C$ TO $85^{\circ}C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-------------|-----------------------------------|-----------------|----------------|---------|----------------|-------|
| V_{OH} | Output High Voltage; NOTE 1 | | $V_{CC} - 1.4$ | | $V_{CC} - 1.0$ | V |
| V_{OL} | Output Low Voltage; NOTE 1 | | $V_{CC} - 2.0$ | | $V_{CC} - 1.7$ | V |
| V_{SWING} | Peak-to-Peak Output Voltage Swing | | 0.6 | | 0.85 | V |

NOTE 1: Outputs terminated with 50Ω to $V_{CCO} - 2V$.

TABLE 5. AC CHARACTERISTICS, $V_{CC} = V_{CCO} = 2.375V$ TO $3.8V$, $T_A = -40^{\circ}C$ TO $85^{\circ}C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|--------------|------------------------------|-----------------|---------|---------|---------|-------|
| f_{MAX} | Output Frequency | | | | 700 | MHz |
| t_{PD} | Propagation Delay; NOTE 1 | $f \leq 500MHz$ | | 2 | 2.5 | ns |
| $t_{sk(o)}$ | Output Skew; NOTE 2, 4 | | | 30 | 55 | ps |
| $t_{sk(pp)}$ | Part-to-Part Skew; NOTE 3, 4 | | | 140 | 340 | ps |
| t_R | Output Rise Time | 20% to 80% | 200 | | 700 | ps |
| t_F | Output Fall Time | 20% to 80% | 200 | | 700 | ps |
| odc | Output Duty Cycle | | 47 | | 53 | % |

All parameters measured at 500MHz unless noted otherwise.

NOTE 1: Measured from the differential input crossing point to the differential output crossing point.

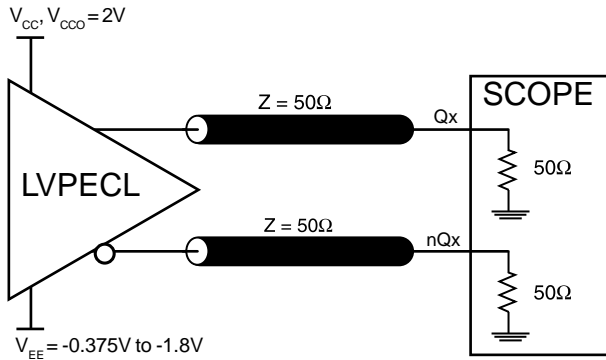
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.

NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

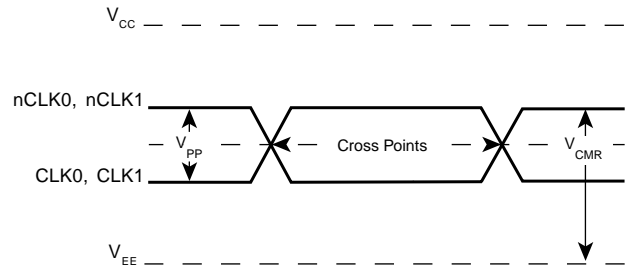
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.



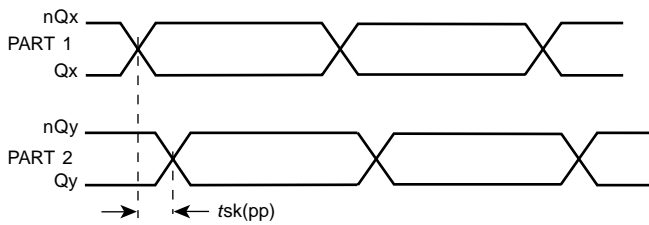
PARAMETER MEASUREMENT INFORMATION



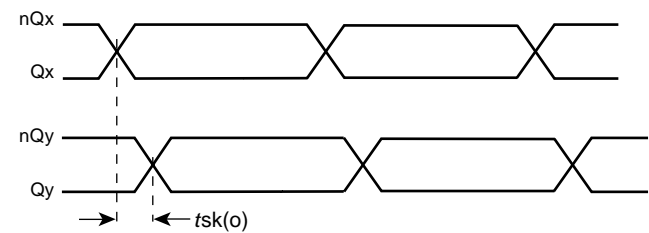
3.3V OUTPUT LOAD AC TEST CIRCUIT



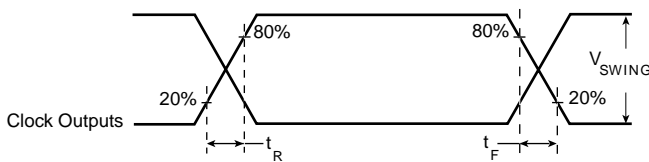
DIFFERENTIAL INPUT LEVEL



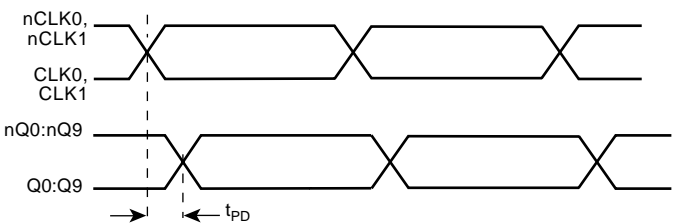
PART-TO-PART SKEW



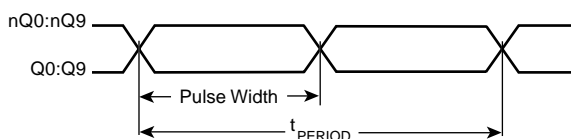
OUTPUT SKEW



OUTPUT RISE/FALL TIME



PROPAGATION DELAY



$$odc = \frac{t_{PW}}{t_{PERIOD}}$$

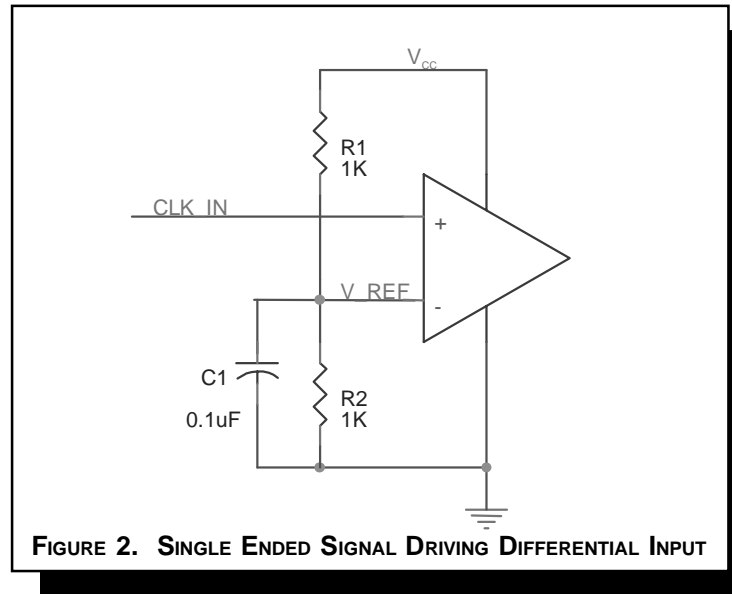
odc & t_{PERIOD}



APPLICATION INFORMATION

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 2 shows how the differential input can be wired to accept single ended levels. The reference voltage $V_{REF} \approx V_{CC}/2$ is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_{REF} in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and $V_{CC} = 3.3V$, V_{REF} should be 1.25V and $R2/R1 = 0.609$.

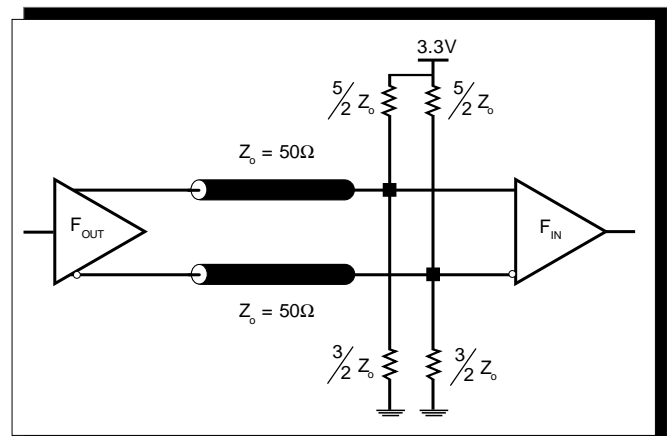
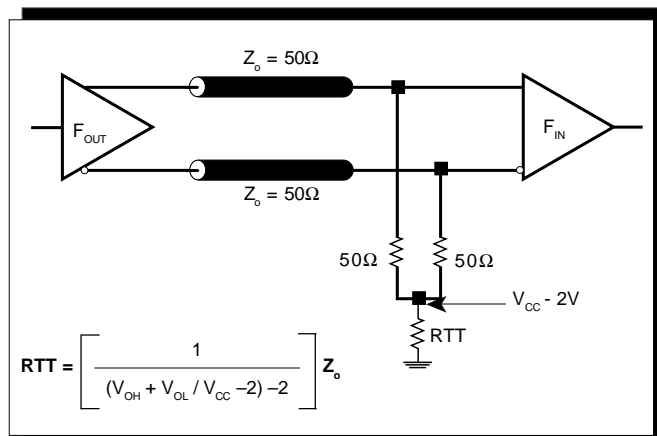


TERMINATION FOR LVPECL OUTPUTS

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive

50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. Figures 3A and 3B show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.





POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS85310I-11. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS85310I-11 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for $V_{CC} = 3.8V$, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)_{MAX} = $V_{CC_MAX} * I_{EE_MAX} = 3.8V * 120mA = 456mW$
- Power (outputs)_{MAX} = **30.2mW/Loaded Output pair**
If all outputs are loaded, the total power is $10 * 30.2mW = 302mW$

Total Power_{MAX} (3.8V, with all outputs switching) = $456mW + 302mW = 758mW$

2. Junction Temperature.

Junction temperature, T_j , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for T_j is as follows: $T_j = \theta_{JA} * Pd_total + T_A$

T_j = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 42.1°C/W per Table 6 below.

Therefore, T_j for an ambient temperature of 85°C with all outputs switching is:

$85°C + 0.758W * 42.1°C/W = 117°C$. This is below the limit of 125°C

This calculation is only an example. T_j will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 6. THERMAL RESISTANCE θ_{JA} FOR 32-PIN LQFP, FORCED CONVECTION

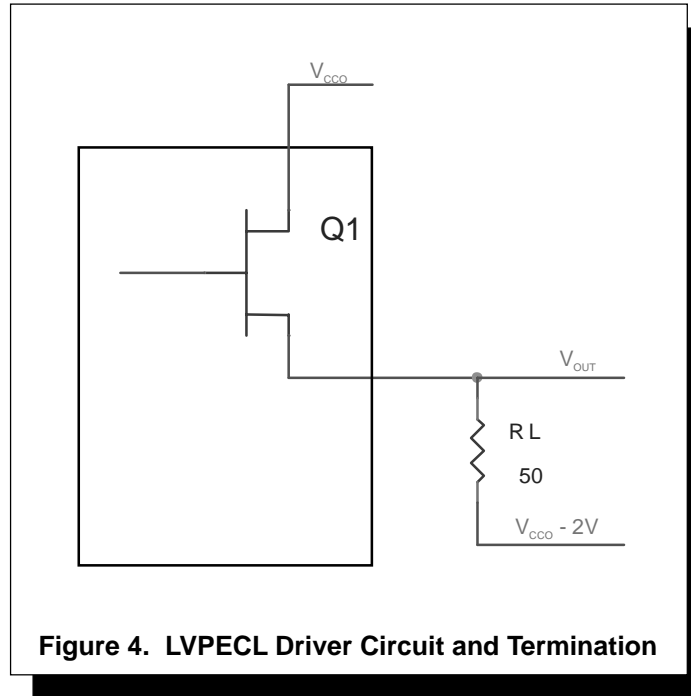
| | θ_{JA} by Velocity (Linear Feet per Minute) | | |
|--|--|----------|----------|
| | 0 | 200 | 500 |
| Single-Layer PCB, JEDEC Standard Test Boards | 67.8°C/W | 55.9°C/W | 50.1°C/W |
| Multi-Layer PCB, JEDEC Standard Test Boards | 47.9°C/W | 42.1°C/W | 39.4°C/W |

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.



3. Calculations and Equations.

LVPECL output driver circuit and termination are shown in Figure 4.



To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of $V_{CCO} - 2V$.

- For logic high, $V_{OUT} = V_{OH_MAX} = V_{CCO_MAX} - 1.0V$

$$(V_{CCO_MAX} - V_{OH_MAX}) = 1.0V$$

- For logic low, $V_{OUT} = V_{OL_MAX} = V_{CCO_MAX} - 1.7V$

$$(V_{CCO_MAX} - V_{OL_MAX}) = 1.7V$$

$$Pd_H = [(V_{OH_MAX} - (V_{CCO_MAX} - 2V))/R_L] * (V_{CCO_MAX} - V_{OH_MAX}) = [(2V - (V_{CCO_MAX} - V_{OH_MAX}))/R_L] * (V_{CCO_MAX} - V_{OH_MAX}) = [(2V - 1V)/50\Omega] * 1V = 20.0mW$$

$$Pd_L = [(V_{OL_MAX} - (V_{CCO_MAX} - 2V))/R_L] * (V_{CCO_MAX} - V_{OL_MAX}) = [(2V - (V_{CCO_MAX} - V_{OL_MAX}))/R_L] * (V_{CCO_MAX} - V_{OL_MAX}) = [(2V - 1.7V)/50\Omega] * 1.7V = 10.2mW$$

Total Power Dissipation per output pair = $Pd_H + Pd_L = 30.2mW$



RELIABILITY INFORMATION

TABLE 7. θ_{JA} VS. AIR FLOW TABLE

| θ_{JA} by Velocity (Linear Feet per Minute) | | | |
|--|----------|----------|----------|
| | 0 | 200 | 500 |
| Single-Layer PCB, JEDEC Standard Test Boards | 67.8°C/W | 55.9°C/W | 50.1°C/W |
| Multi-Layer PCB, JEDEC Standard Test Boards | 47.9°C/W | 42.1°C/W | 39.4°C/W |

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS85310I-11 is: 1034



PACKAGE OUTLINE - Y SUFFIX

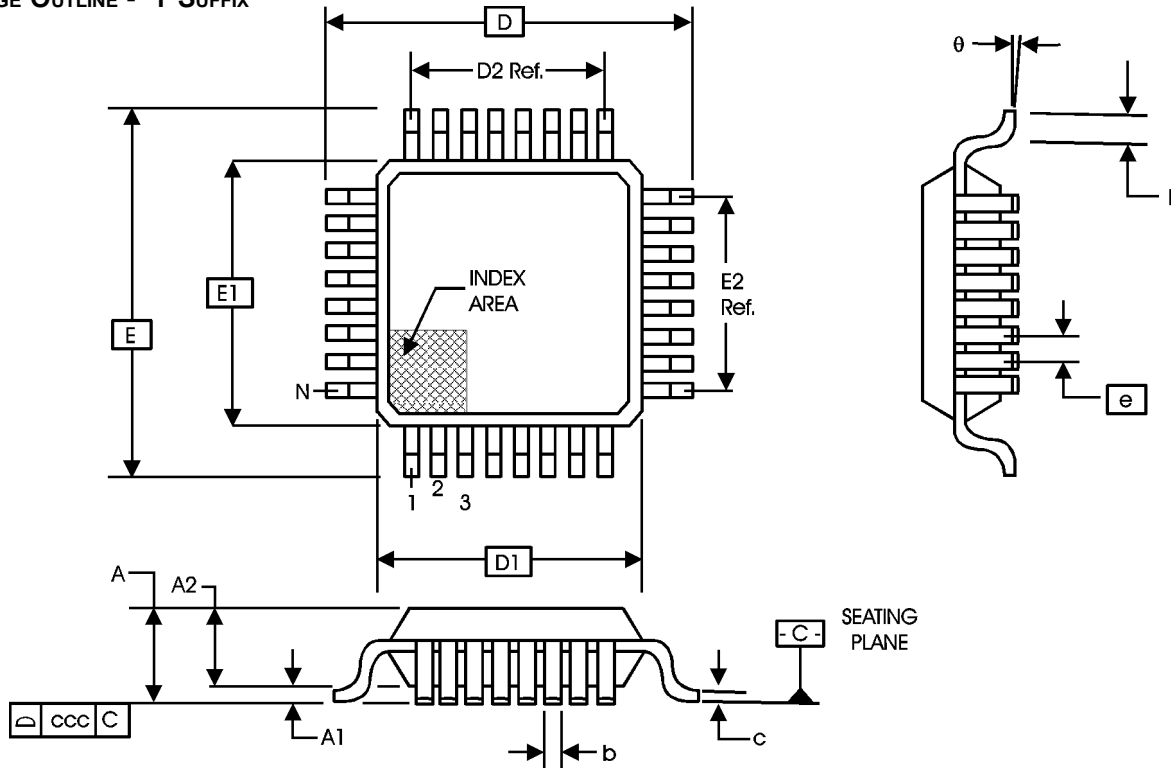


TABLE 8. PACKAGE DIMENSIONS

| JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS | | | |
|--|------------|---------|---------|
| SYMBOL | BBA | | |
| | MINIMUM | NOMINAL | MAXIMUM |
| N | 32 | | |
| A | -- | -- | 1.60 |
| A1 | 0.05 | -- | 0.15 |
| A2 | 1.35 | 1.40 | 1.45 |
| b | 0.30 | 0.37 | 0.45 |
| c | 0.09 | -- | 0.20 |
| D | 9.00 BASIC | | |
| D1 | 7.00 BASIC | | |
| D2 | 5.60 Ref. | | |
| E | 9.00 BASIC | | |
| E1 | 7.00 BASIC | | |
| E2 | 5.60 Ref. | | |
| e | 0.80 BASIC | | |
| L | 0.45 | 0.60 | 0.75 |
| θ | 0° | -- | 7° |
| ccc | -- | -- | 0.10 |

Reference Document: JEDEC Publication 95, MS-026



Integrated
Circuit
Systems, Inc.

ICS85310I-11

LOW SKEW, 1-TO-10
DIFFERENTIAL-TO-2.5V/3.3V ECL/LVPECL FANOUT BUFFER

TABLE 9. ORDERING INFORMATION

| Part/Order Number | Marking | Package | Count | Temperature |
|-------------------|---------------|-------------------------------|--------------|---------------|
| ICS85310AYI-11 | ICS85310AYI11 | 32 lead LQFP | 250 per tray | -40°C to 85°C |
| ICS85310AYI-11T | ICS85310AYI11 | 32 lead LQFP on Tape and Reel | 1000 | -40°C to 85°C |

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ICS85310I-11

LOW SKEW, 1-TO-10

DIFFERENTIAL-TO-2.5V/3.3V ECL/LVPECL FANOUT BUFFER

| REVISION HISTORY SHEET | | | | |
|------------------------|-------|------|--|----------|
| Rev | Table | Page | Description of Change | Date |
| B | T5 | 5 | AC Characteristics table - t_{PD} row, revised value from 2.25ns Max. to 2.5ns Max. | 4/29/02 |
| | | 9 | Added Termination for LVPECL Outputs section. | 5/29/02 |
| C | 4D | 5 | Added LVPECL DC Characteristics table. Changed part number from ICS85310-11 to ICS85310I-11 in title and all subsequent areas throughout the datasheet. | 7/25/02 |
| | | 4 | Power Supply table - increased max. value for I_{EE} to 120mA from 30mA max. | 10/23/02 |
| D | T4A | 10 | Power Considerations have re-adjusted to the increased I_{EE} value. | |